IN THE CLAIMS

The text of all pending claims, along with their current status, is set forth below:

1. (Previously Presented) A processor having a normal mode and a speculative prefetching mode, the processor operable in the speculative prefetching mode after a data cache miss, comprising:

a first data cache for storing data when the processor operates in the normal mode;

a second data cache for storing data in response to a store instruction when the processor operates in the speculative prefetching mode;

a first program counter for use when the processor operates in the normal mode; and

a second program counter for use only when the processor operates in the speculative prefetching mode, wherein the first program counter is configured to remain unchanged during operation of the processor in the speculative prefetching mode.

2. (Original) The processor of claim 1, wherein the second data cache comprises:

an entry for storing data; and

a trash bit associated with the entry, wherein the trash bit indicates whether the entry contains arbitrary data.

3-9. (Canceled).

10. (Original) The processor of claim 1, wherein the first data cache comprises a direct-mapped cache and where the second data cache comprises an associative cache.

11. (Previously Presented) A processor having a normal mode and a speculative prefetching mode, the processor operable in the speculative prefetching mode after a data cache miss, comprising:

a first register for storing data during the normal mode;

a second register for storing data during the speculative prefetching mode, the second register comprising a first trash bit that indicates whether the second register contains arbitrary data;

a first program counter for use when the processor operates in the normal mode;

a second program counter for use only when the processor operates in the speculative prefetching mode, wherein the first program counter is configured to remain unchanged during operation of the processor in the speculative prefetching mode;

an instruction bus for receiving a stream of instructions including a first instruction and a second instruction;

control logic for executing the first instruction;

control logic for initiating a cache fill request provided execution of the first instruction encounters a data cache miss;

control logic for setting the trash bit of the second register in response to the first instruction and the data cache miss; and

control logic for executing the second instruction in the speculative prefetching mode using the second register in place of the first register.

12. (Original) The processor of claim 11, further comprising:

a first data cache for storing data during the normal model; and

a second data cache for storing data in response to a store instruction during the speculative prefetching mode.

13. (Original) The processor of claim 12, wherein the second data cache comprises:

an entry for storing data; and

a second trash bit associated with the entry, the second trash bit for indicating whether the entry contains arbitrary data.

14-18 (Canceled).

19. (Original) The processor of claim 11, wherein the first data cache is a direct-mapped cache and the second data cache is an associative cache.

20-22. (Canceled).

23. (Previously Presented) The processor of claim 1, including logic for continuing to execute a program after a data cache miss, in the speculative prefetching mode, using the second program counter and the second data cache, leaving the first data cache and the first program counter unchanged during execution of the program in the speculative prefetching mode.

24. (Cancelled)

25. (New) A processor having a normal mode and a speculative prefetching mode, the processor operable in the speculative prefetching mode after a data cache miss, comprising:

a first register for storing data during the normal mode;

a second register for storing data during the speculative prefetching mode, the second register comprising a first trash bit that indicates whether the second register contains arbitrary data and a first valid bit that indicates whether the second register is in use.

a first program counter for use when the processor operates in the normal mode;

a second program counter for use only when the processor operates in the speculative prefetching mode, wherein the first program counter is configured to remain unchanged during operation of the processor in the speculative prefetching mode;

an instruction bus for receiving a stream of instructions including a first instruction and a second instruction;

control logic for executing the first instruction;

control logic for initiating a cache fill request provided execution of the first instruction encounters a data cache miss;

control logic for setting the trash bit of the second register in response to the first instruction and the data cache miss; and

control logic for executing the second instruction in the speculative prefetching mode using the second register in place of the first register.